Fermi National Accelerator Laboratory

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A FAST PROCESSOR FOR DILEPTON TRIGGERS*

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We describe a fast trigger processor, developed for and used in Fermilab experiment E-537, for selecting high-mass dimuon events produced by negative pions and anti-protons. The processor finds candidate tracks by matching hit information received from drift chambers and scintillation counters, and determines their momenta. Invariant masses are calculated for all possible pairs of tracks and an event is accepted if any invariant mass is greater than some preselectable minimum mass. The whole process, accomplished within 5 to 10 microseconds, achieves up to a ten-fold reduction in trigger rate.

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1. Introduction

A magnetic spectrometer utilizing drift chambers and scintillation counters was built at Fermilab in order to study high mass dimuon ($M_{\mu^+\mu^-} \geq 3$ GeV/c^2) production by 125 GeV/c antiprotons and negative pions [1]. The basic dimuon trigger rate was dominated by low mass events and at the desired beam intensity well exceeded the ability of the data acquisition system to record events efficiently. To solve this problem, a fast digital processor was designed and built in order to filter out background or low mass triggers prior to the recording of data.

The hardware of this processor consisted of two parts, a fast encoder followed by a difital processor. Both parts used ECL circuitry throughout. The encoder latched the hit information from ≈ 600 detector channels and encoded a selected subset of this information into binary numbers. The processor then operated on these numbers to determine the validity of the event. The encoder system was an entirely new design; the processor was a new application of the Fermilab ECL-CAMAC system [2].

2. The Experiment

The experimental apparatus is shown in Fig. 1. More detailed description of the apparatus and the experiment may be found in Refs. 3 and 4. A negative beam enriched in anti-protons from $\bar{\Lambda} \rightarrow \bar{p}\pi^+$ decays [5] was tagged by Cerenkov and scintillation counters and momentum analyzed by a set of multi-wire proportional chambers. A 1.5m long copper absorber followed the 1 or 1.5 interaction lengths of the nuclear target. Drift chambers, upstream and downstream of a large aperture analysis magnet, measured the momenta of the charged particles surviving the absorber. Scintillation counters,

(charged particle hodoscopes CPX and CPY) situated behind the last drift chamber provided further tagging in horizontal and vertical directions. Muon identification was provided by a hodoscope consisting of three planes of scintillation counters (60 per plane), embedded in 350 tons of steel and concrete. A muon produced at the target was identified by a triple coincidence among suitably aligned counters in the three planes. The fast logic trigger required a beam particle in coincidence with at least two hits in the CPX hodoscope and muon triple coincidences from two different quadrants of the muon hodoscope.

In addition to spurious triggers, (due to the beam halo, decay muons and hadron punch-through), a large class of unwanted triggers arose from the spectrum of low mass dimuons ($M_{\mu^+\mu^-}<3$ GeV/c^2), which dominates the dimuon cross section. Most of the schemes suppressing such contributions also decrease and distort the acceptance of high mass events. In an experiment making an absolute measurement of a small cross section, it is essential to minimize the loss and distortion of data. The most preferable way of filtering the triggers is a true dimuon mass calculation. The trigger processor scheme for the experiment was designed to provide a fast and good resolution calculation of dimuon mass.

3. General Scheme of the Processor

In this section, some important concepts, assumptions and approximations made in building the processor are described. Figure 2 shows the processor's view of the experiment. The magnetic field was represented by a bend plane and a point interaction vertex was assumed at the physical centre of the target. No track finding was done upstream of the magnet, while downstream of the magnet information from the x-planes of the drift chambers and the CPX, CPY and muon hodoscopes was used in track searching. Relevant para-

it would be if no road conditions were imposed. Table 2 shows the number of wires and counters involved in the narrowest and widest roads of the experimental setup.

4. Interface to the Processor

Fig. 4 shows the block diagram of the fast encoder that interfaces the experiment to the ECL-CAMAC processor. The tasks of the fast encoder are

a) to receive and store all the hit information from the relevant detectors, and

b) to organize the drift chamber and CPX data by roads and present them to the processor, one road at a time.

The muon triple coincidences (defining the roads) were latched in a Road Address Encoder Module (ROAD ENCODER). Available at the output ports of this module were the number of the road (absolute road number) and a sequential number (sequential road number) that uniquely identified each road. The information regarding which detector elements were relevant for the current road was stored in a set of Memory Pattern Storage Modules (MPSMs). The MPSM contained RAMs arranged in 3 banks, each bank capable of storing 16 bit words (memory patterns) in 256 different locations. Memory patterns stored in any location in all 3 banks could be brought out by presenting the proper address (in our case, the absolute road number) to the MPSM. Thus, a memory pattern could be as wide as 48 bits. The drift chamber, CPX and CPY hit information was latched in a set of Wire/Counter Number Encoder Modules (HIT ENCODERS). The Hit Encoder stored, in sixteen 4 bit latches, the data present at its inputs during the trigger gate. The data stored in this module could be overwritten only by a subsequent event trigger. A memory pattern presented to the hit encoder caused the subset of the stored data

roads had been processed, this module terminated data transmission to the processor.

5. The ECL-CAMAC processor

The ECL-CAMAC trigger processor system was developed at Fermilab for event filtering prior to online data acquisition. The system consists of general utility logic and arithmetic modules, built of fast ECL integrated circuits. CAMAC like crates, where the modules reside, have modified back planes for carrying ECL signals. Each crate communicates with the host computer via a standard type A-1 crate controller. A translator module, in station 23 of each crate, converts the CAMAC TTL signals to ECL and transmits them to the rest of the crate.

Front panel connectors, carrying ECL differential signals on twist and flat ribbon or shielded 2-pin twisted pair cables, link individual modules to each other. This feature allows easy reconfiguration of the system or function redefinition of any module. One key element of the system is the Memory Look Up module (MLU), containing 16 x 4K (or 16 x 1K) ECL RAMs, with roughly 50 nanosecond access time. Pre-computed tables of logical or arithmetic functions stored in these modules via CAMAC dataway are accessed during run time through front panel address ports, resulting in a fast computational capability. An important feature of the system is its asynchronous operation; each module when activated by a set of input ready lines, produces an output ready signal, facilitating parallel processing and flow optimization of tasks that require different times for completion.

A simplified block diagram of the processor is shown in Fig. 6 and the associated logic flow is shown in Fig. 7. Detailed description of the modules appearing in the diagram and mentioned in the text may be found in Ref. 2.

greater than 4 GeV, since a muon originating at the target required at least 5.5 GeV of energy in order to be detected at the last muon plane. In parallel, two other MLUs projected the track to the CPX and muon hodoscopes and computed the addresses of the counters that should be hit. The CPX counter number was presented as an examining address to the Hit Array Module, which responded with either a 'match' or a 'no match' output bit depending on the set value at that location. The muon counter number was compared with the road address (absolute road number) available form the Road Encoder. A good track which had the proper energy and matching hits in the CPX and muon hodoscopes was tagged with a 3-bit sequential road number and was stored in a set of two Stacks. The sequential road number was useful in avoiding pairing tracks from the same road during mass computation. Good tracks from the second road were written into another set of two Stacks. In the less frequent case of events with greater than two good roads, tracks from the third and subsequent roads were written into both sets of Stacks. This procedure was a good compromise between keeping down the number of required Stacks (to store tracks from different roads) and minimizing unnecessary track pairings during mass computation.

Track verification began as soon as the first candidate track was written into the buffer and continued in parallel with track finding. Typical time for validating a single track was approximately 200 nanoseconds.

c) Calculation of Y Opening Angle: This stage was completely independent of the other stages and began when the data from the CPY HECM was available. In the current Trigger Processor implementation, the hits from the pair of counters that were furthest apart were used to calculate the vertical opening angle θ_y.

software simulator, thus completely testing our scheme.

Two test modules, one storing the wire chamber and the muon hodoscope data and the other the CPX and CPY hodoscope data, were developed to allow testing the processor in its designed configuration. These units, loaded with fake events via the CAMAC dataway, presented the trigger processor with data at a rate comparable to that of the HECMs. Concurrently with the assembly of the processor, a diagnostics/simulator program using the interactive language FORTH [6] was developed. By means of this program, increasingly complex events were presented to the processor, therby gradually debugging its operations. Finally, the test modules were loaded with real events from data tapes. On an event-by-event basis, the processor's results at various stages were compared with the results obtained by feeding the same data to the software simulator.

Prior to integrating the processor into the experiment, its real time performance was monitored during normal data taking runs. The results are shown in Fig. 8. During the experiment, the processor's performance was monitored in the following way. At pre-scaled intervals, the processor's control over data taking was inhibited and its response to the event was recorded. The processor's stacks were then read out and verified against the software stacks in the online simulator. Since only a fraction of all pre-scaled events could be analyzed online, these events were written to tape for further offline verification of the trigger processor's performance.

The decision time of the processor was between 5 and 10 microseconds per event. By setting the mass cut-off value at 2 GeV/c^2, the trigger rate was reduced by a factor between 5 and 10, the actual figure depending on the specific beam and trigger conditions. The efficiency for recording

8. Acknowledgments

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TABLE 1

Detector Parameters

Detector name	Detector type	Number of elements	Cell or Counter dimension	Total area covered
DWC 4	Drift chamber	124	2 x 118 cm^2	2.9 m^2
DWC 5	Drift chamber	176	2 x 168 cm^2	5.9 m^2
DWC 6	Drift chamber	176	2 x 168 cm^2	5.9 m^2
CPX	Scintillation counter hodoscope	184	4 x 100 cm^2	7.4 m^2
CPY	Scintillation counter hodoscope	48	8 x 200 cm^2	7.7 m^2
H_1	Scintillation counter hodoscope	60	20 x 145 cm^2	17.4 m^2

TABLE 2

Number of detector elements in the narrowest and widest roads

	No. of elements			
	DWC 4	DWC 5	DWC 6	CPX
Narrowest road	32	32	20	12
Widest road	64	52	48	28

Figure Captions

1. E-537 spectrometer.

2a. Trigger Processor's view of the experiment; XZ plane.

2b. Trigger Processor's view of the experiment; YZ plane.

3. Track finding efficiency as a function of drift chamber efficiencies.

4. Block diagram of the fast encoder.

5. Simplified diagram of the Hit Encoder.

6. Simplified block diagram of the Trigger Processor.

7. Logic flow of the Trigger Processor.

8. Performance results of the Trigger Processor.

9. Efficiency of the Trigger Processor for events with $M_{\mu^+\mu^-} > 2.5$ GeV/c^2, when mass cut-off value was 2 GeV/c^2.

10. Mass resolution of the Trigger Processor.

11. Mass spectrum of dimuon events for $\bar{p}N$ interactions: Trigger Processor active.

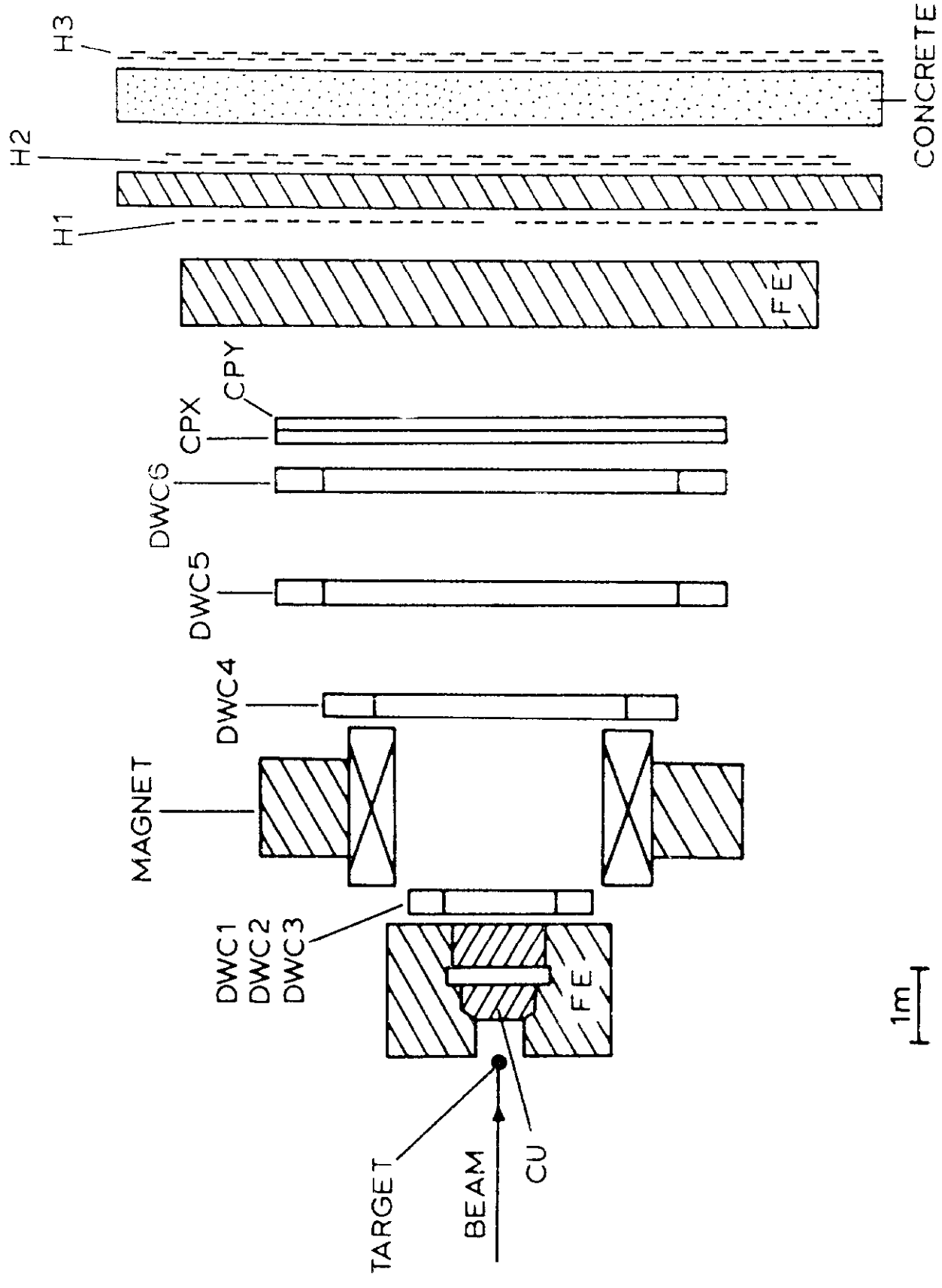
H3
CONCRETE
H2
H1
FE
CPY
CPX
DWC6
DWC5
DWC4
MAGNET
DWC1
DWC2
DWC3
FE
1m
TARGET
BEAM
CU

Fig. 1

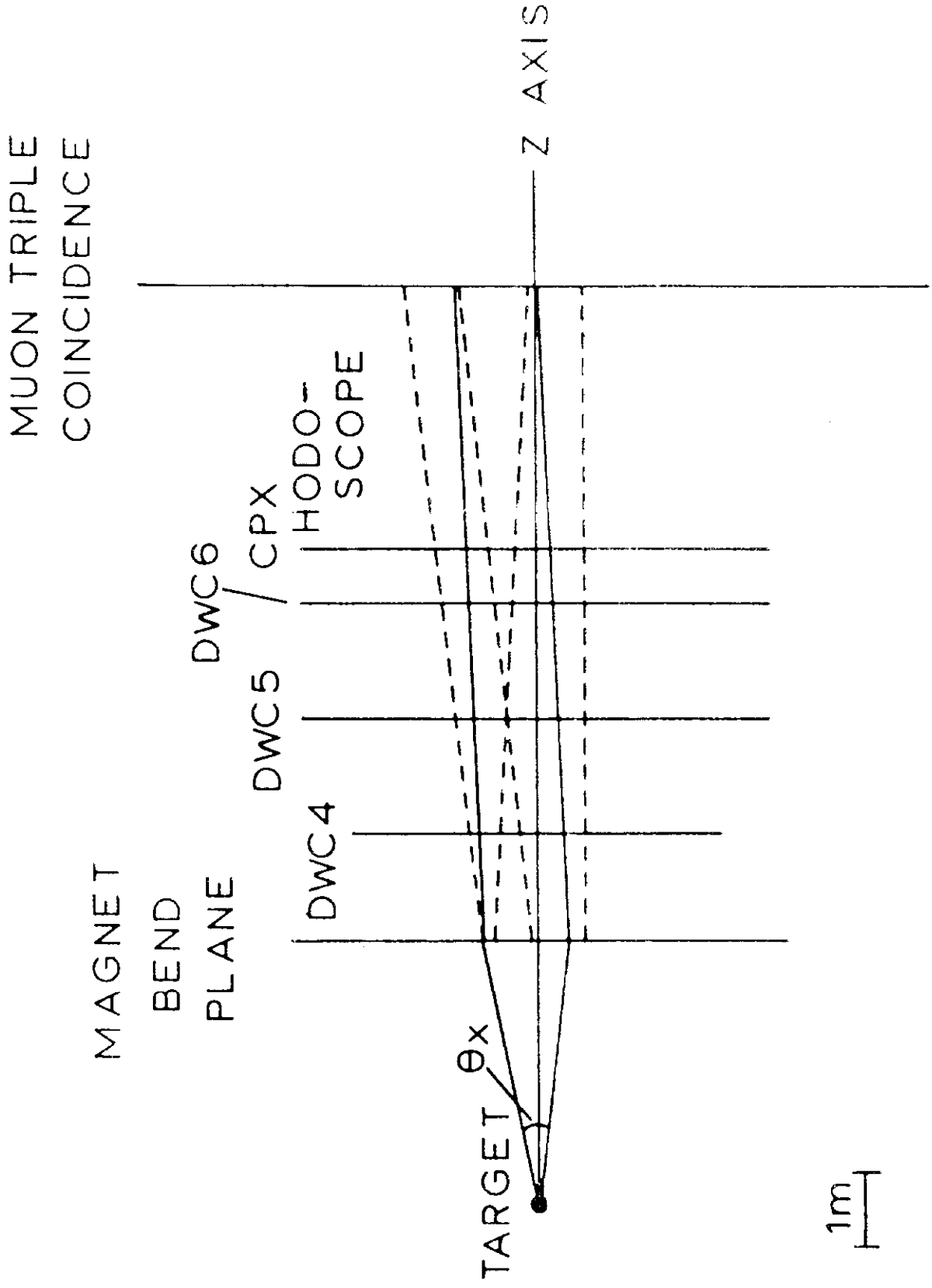
MUON TRIPLE
COINCIDENCE
Z AXIS
HODO-
SCOPE
CPX
DWC6
DWC5
DWC4
MAGNET
BEND
PLANE
θx
TARGET
1m

Fig. 2(a)

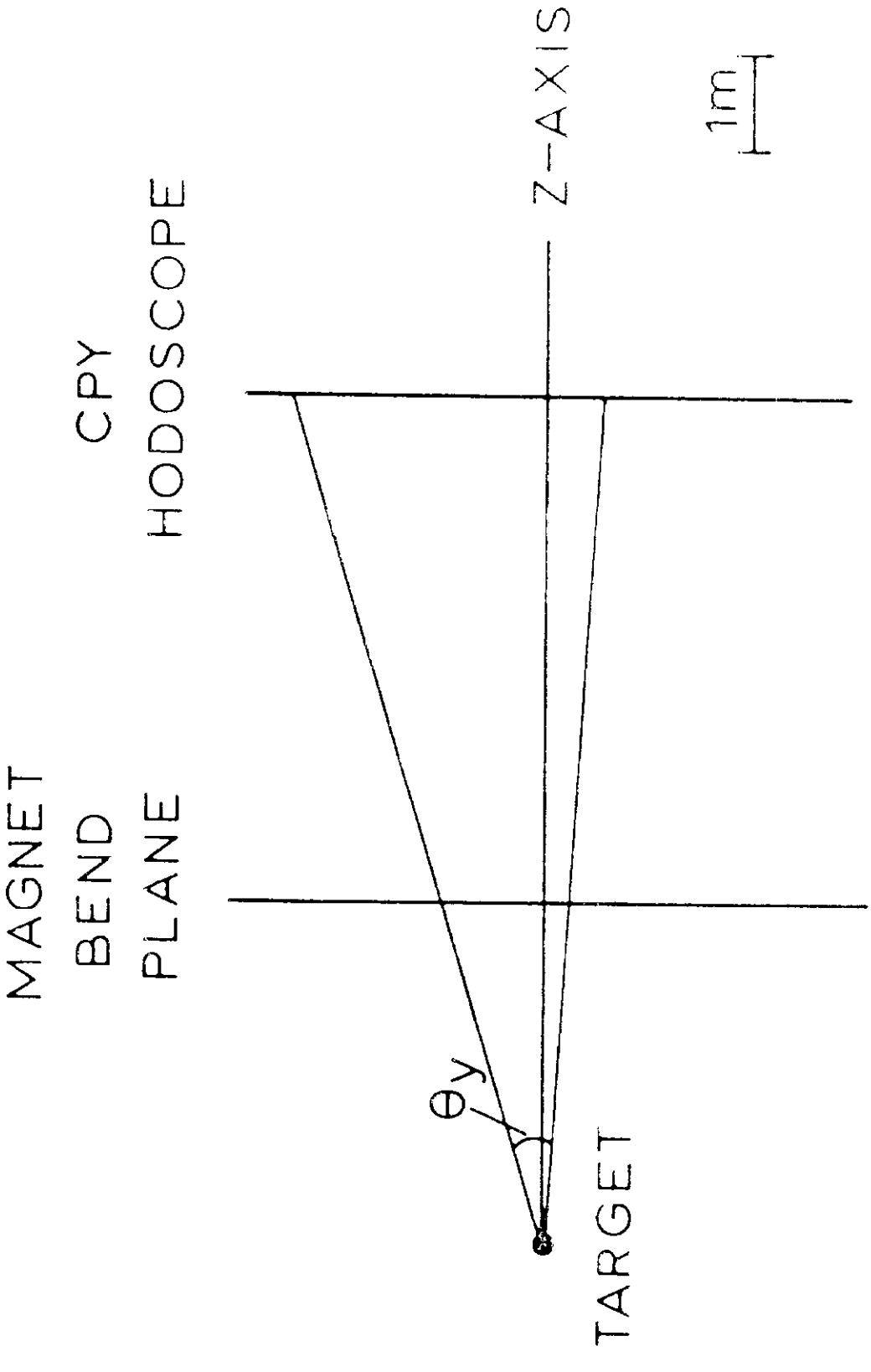

Fig. 2(b)

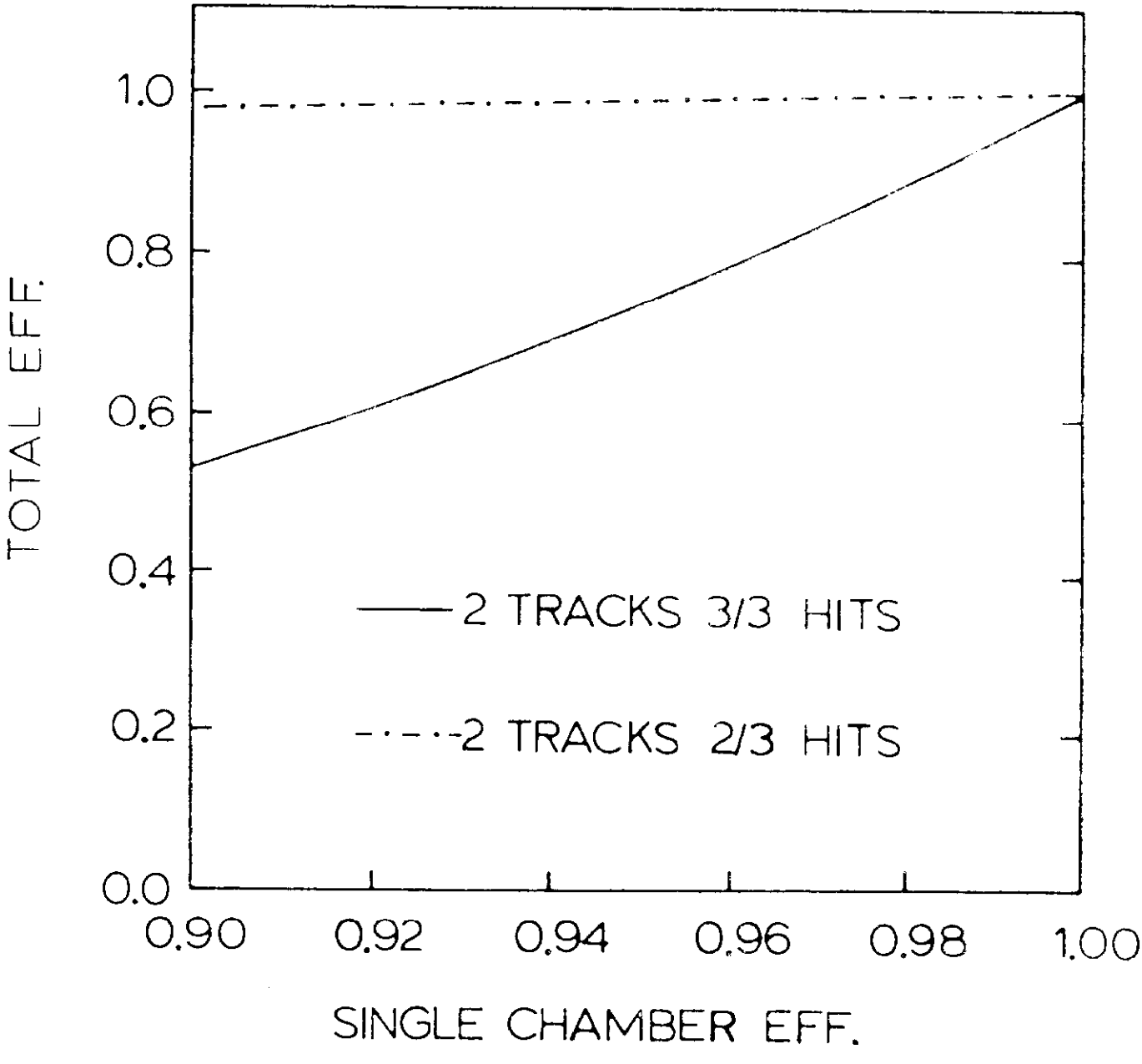
TOTAL EFF.
1.0
0.8
0.6
0.4
0.2
0.0
2 TRACKS 3/3 HITS
2 TRACKS 2/3 HITS
0.90
0.92
0.94
0.96
0.98
1.00
SINGLE CHAMBER EFF.

Fig. 3

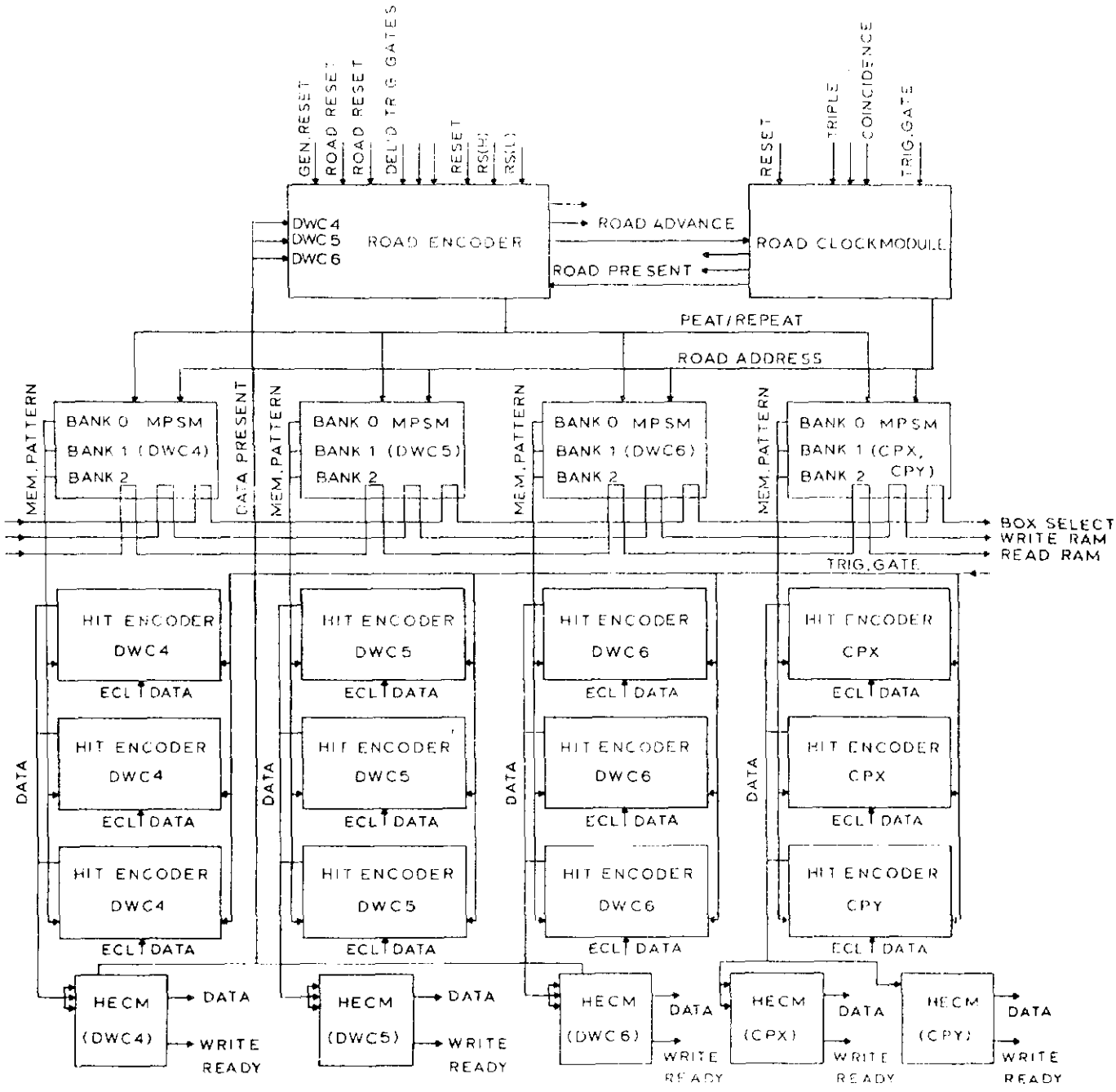
GEN.RESET
ROAD RESET
ROAD RESET
DEL'D TR G GATES
RESET
RS(H)
RS(L)
RESET
TRIPLE
COINCIDENCE
TRIG.GATE
DWC4
DWC5
DWC6
ROAD ENCODER
ROAD ADVANCE
ROAD PRESENT
ROAD CLOCKMODULE
PEAT/REPEAT
ROAD ADDRESS
MEM.PATTERN
BANK 0 MPSM
BANK 1 (DWC4)
BANK 2
DATA PRESENT
MEM.PATTERN
BANK 0 MPSM
BANK 1 (DWC5)
BANK 2
MEM.PATTERN
BANK 0 MPSM
BANK 1 (DWC6)
BANK 2
MEM.PATTERN
BANK 0 MPSM
BANK 1 (CPX,
BANK 2 CPY)
BOX SELECT
WRITE RAM
READ RAM
TRIG.GATE
HIT ENCODER DWC4
HIT ENCODER DWC5
HIT ENCODER DWC6
HIT ENCODER CPX
HIT ENCODER DWC4
HIT ENCODER DWC5
HIT ENCODER DWC6
HIT ENCODER CPX
HIT ENCODER DWC4
HIT ENCODER DWC5
HIT ENCODER DWC6
HIT ENCODER CPY
ECL DATA
DATA
HECM (DWC4)
HECM (DWC5)
HECM (DWC6)
HECM (CPX)
HECM (CPY)
DATA
WRITE READY

Fig. 4

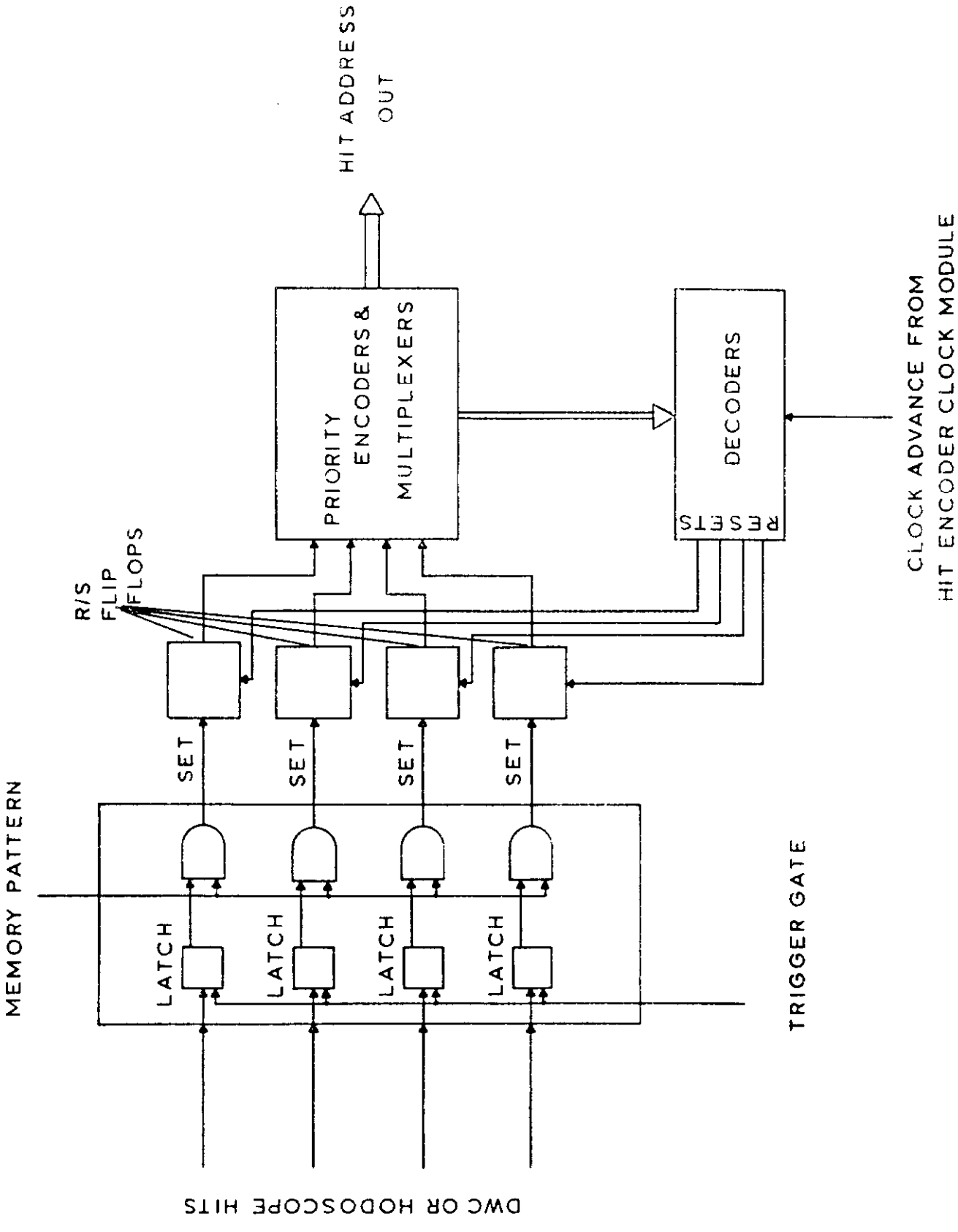
HIT ADDRESS OUT
PRIORITY ENCODERS & MULTIPLEXERS
DECODERS
RESETS
CLOCK ADVANCE FROM HIT ENCODER CLOCK MODULE
R/S FLIP FLOPS
SET
SET
SET
SET
MEMORY PATTERN
LATCH
LATCH
LATCH
LATCH
TRIGGER GATE
DWC OR HODOSCOPE HITS

Fig. 5

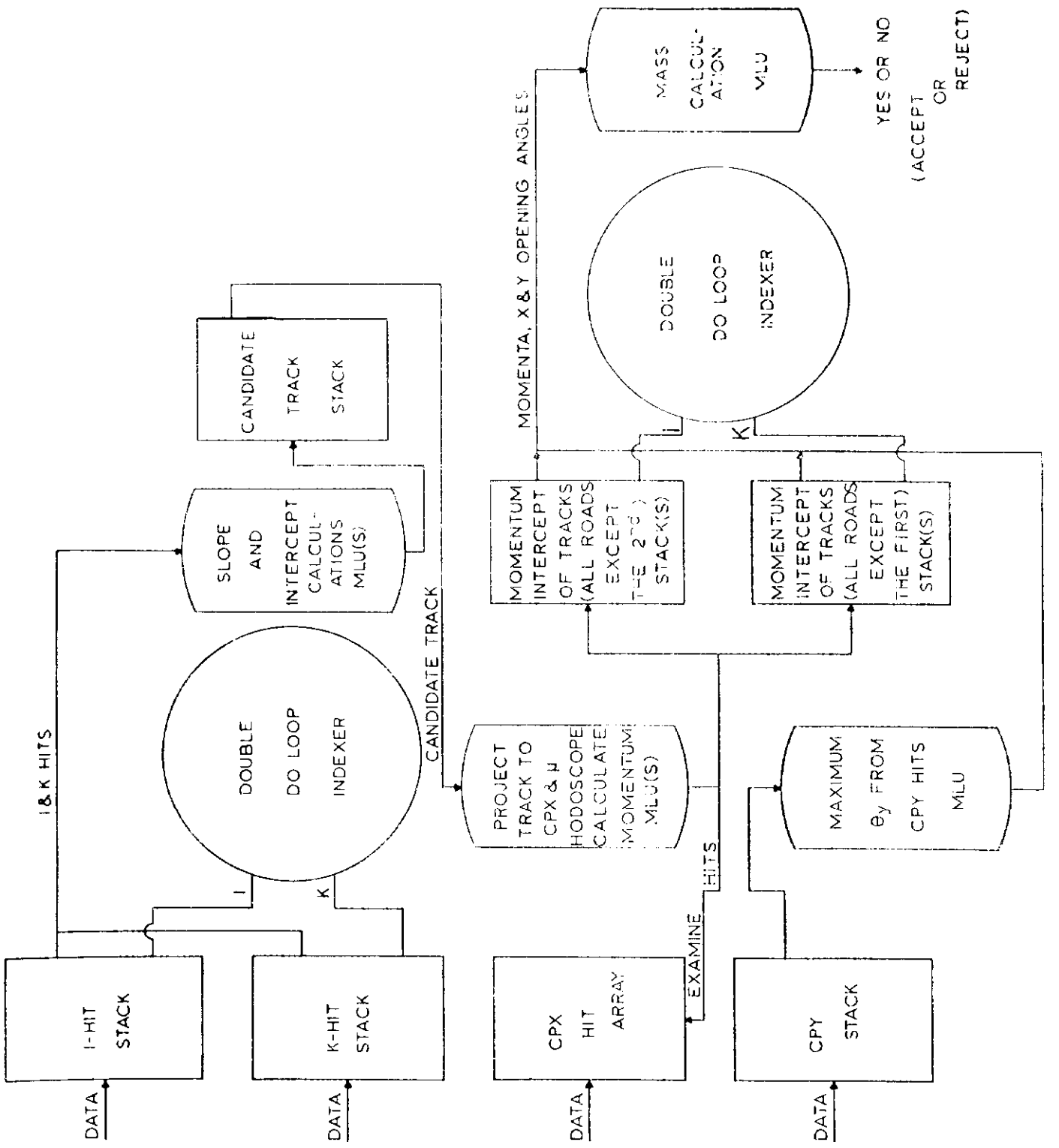
I-HIT STACK
K-HIT STACK
CPX HIT ARRAY
CPY STACK
DATA
DATA
DATA
DATA
I & K HITS
DOUBLE DO LOOP INDEXER
I
K
SLOPE AND INTERCEPT CALCULATIONS MLU(S)
CANDIDATE TRACK STACK
CANDIDATE TRACK
PROJECT TRACK TO CPX & μ HODOSCOPE CALCULATE MOMENTUM MLU(S)
EXAMINE HITS
MOMENTUM INTERCEPT OF TRACKS (ALL ROADS EXCEPT THE 2ND) STACK(S)
MOMENTUM INTERCEPT OF TRACKS (ALL ROADS EXCEPT THE FIRST) STACK(S)
MAXIMUM e_y FROM CPY HITS MLU
MOMENTA, X & Y OPENING ANGLES
DOUBLE DO LOOP INDEXER
I
K
MASS CALCULATION MLU
YES OR NO (ACCEPT OR REJECT)

Fig. 6

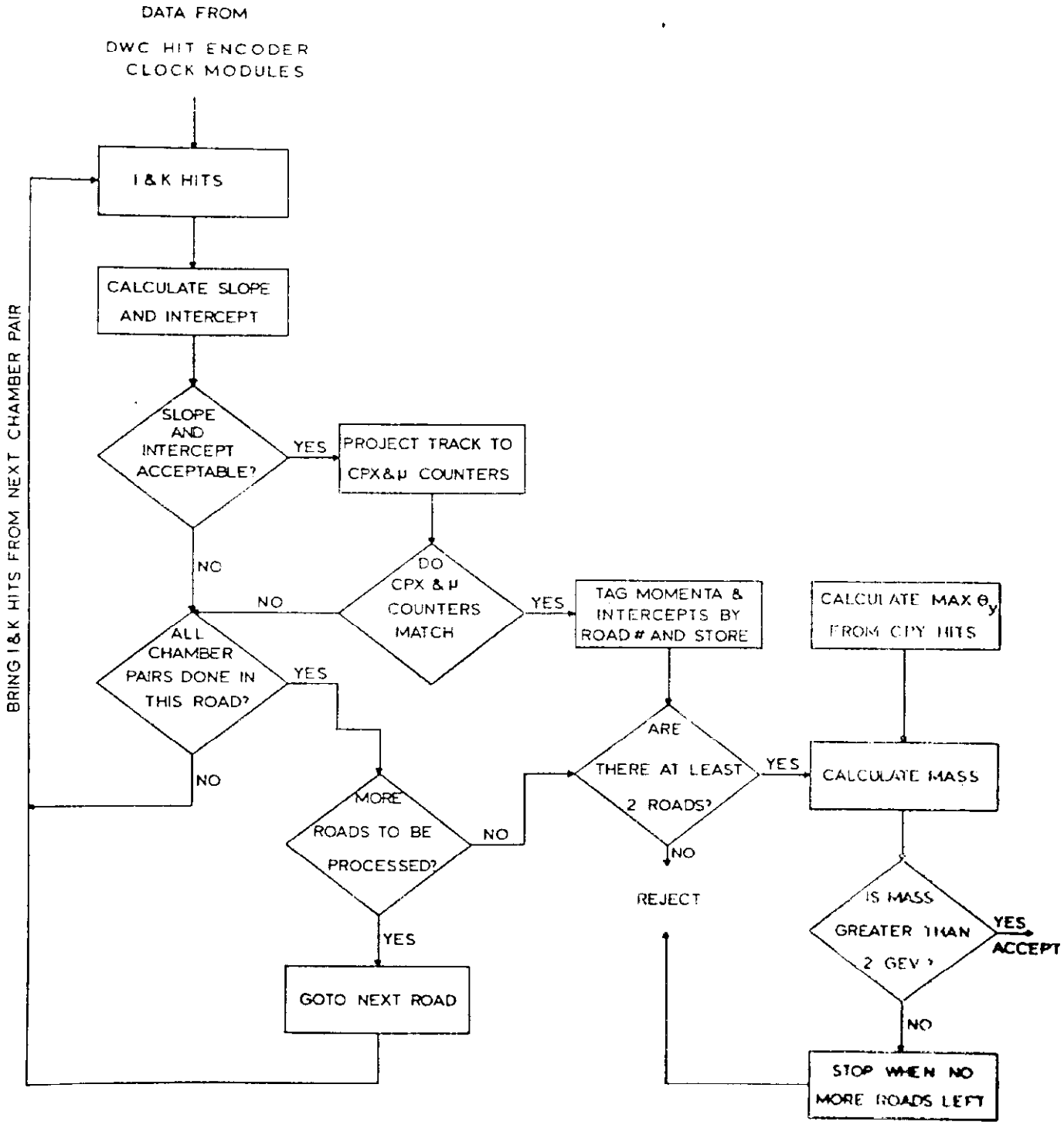
DATA FROM
DWC HIT ENCODER
CLOCK MODULES
I&K HITS
CALCULATE SLOPE
AND INTERCEPT
SLOPE
AND
INTERCEPT
ACCEPTABLE?
YES
PROJECT TRACK TO
CPX&μ COUNTERS
NO
DO
CPX & μ
COUNTERS
MATCH
NO
YES
TAG MOMENTA &
INTERCEPTS BY
ROAD # AND STORE
CALCULATE MAX θ_y
FROM CPY HITS
ALL
CHAMBER
PAIRS DONE IN
THIS ROAD?
YES
NO
ARE
THERE AT LEAST
2 ROADS?
YES
CALCULATE MASS
MORE
ROADS TO BE
PROCESSED?
NO
NO
REJECT
YES
GOTO NEXT ROAD
IS MASS
GREATER THAN
2 GEV ?
YES
ACCEPT
NO
STOP WHEN NO
MORE ROADS LEFT
BRING I&K HITS FROM NEXT CHAMBER PAIR

Fig. 7

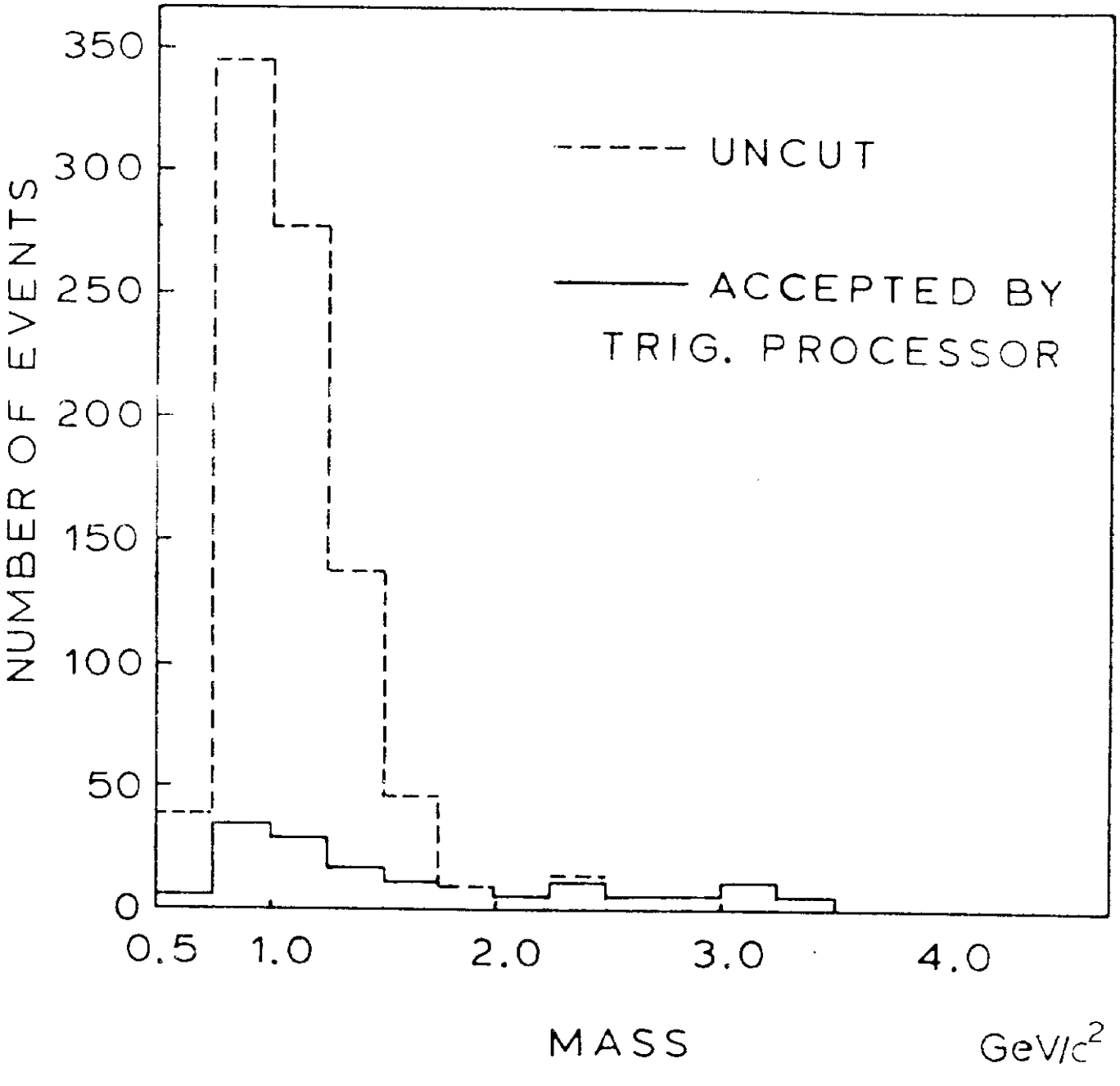
NUMBER OF EVENTS
350
300
250
200
150
100
50
0
0.5
1.0
2.0
3.0
4.0
MASS
GeV/c²
UNCUT
ACCEPTED BY
TRIG. PROCESSOR

Fig. 8

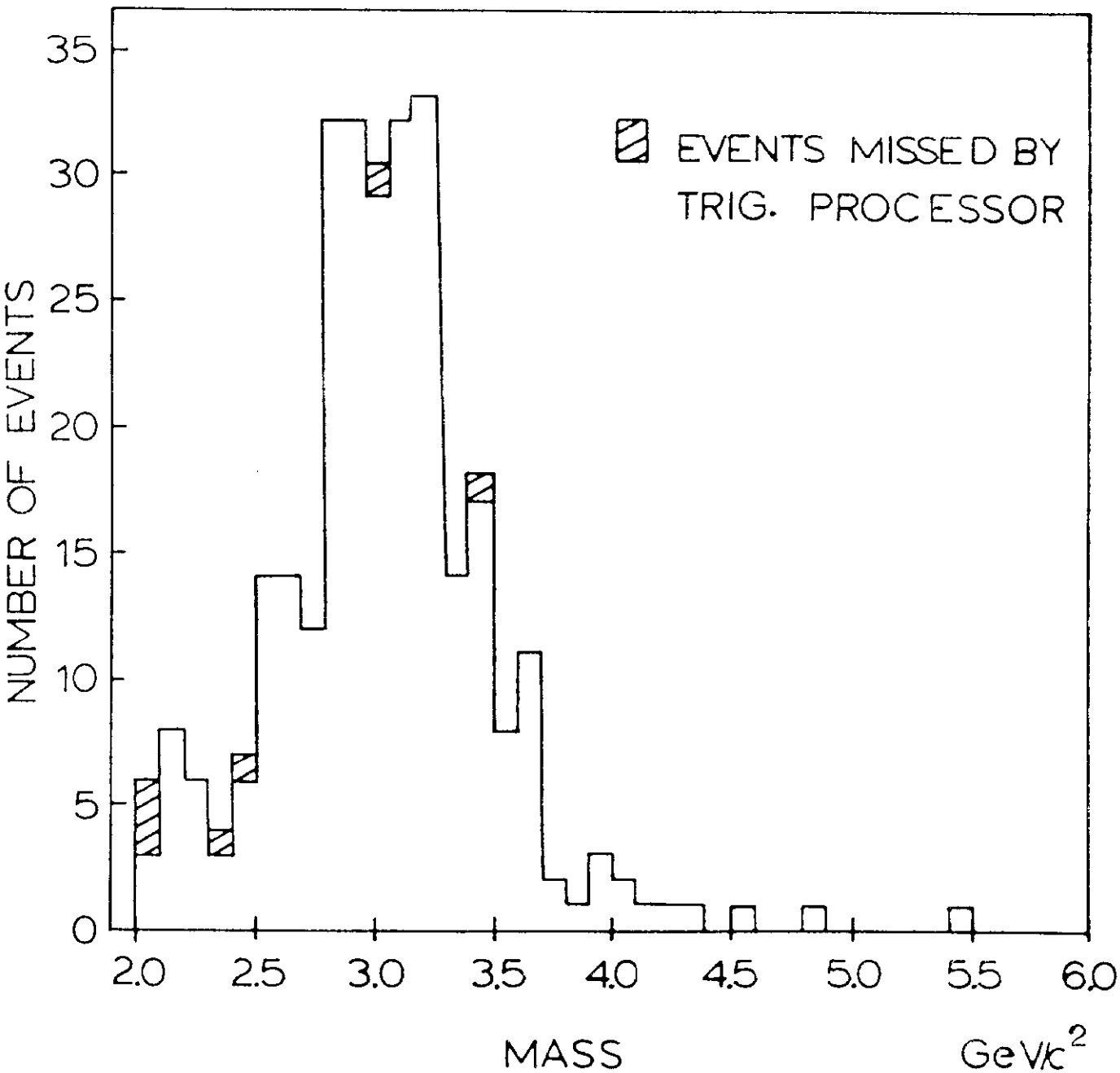
NUMBER OF EVENTS
35
30
25
20
15
10
5
0
EVENTS MISSED BY
TRIG. PROCESSOR
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
MASS
GeV/c²

Fig. 9

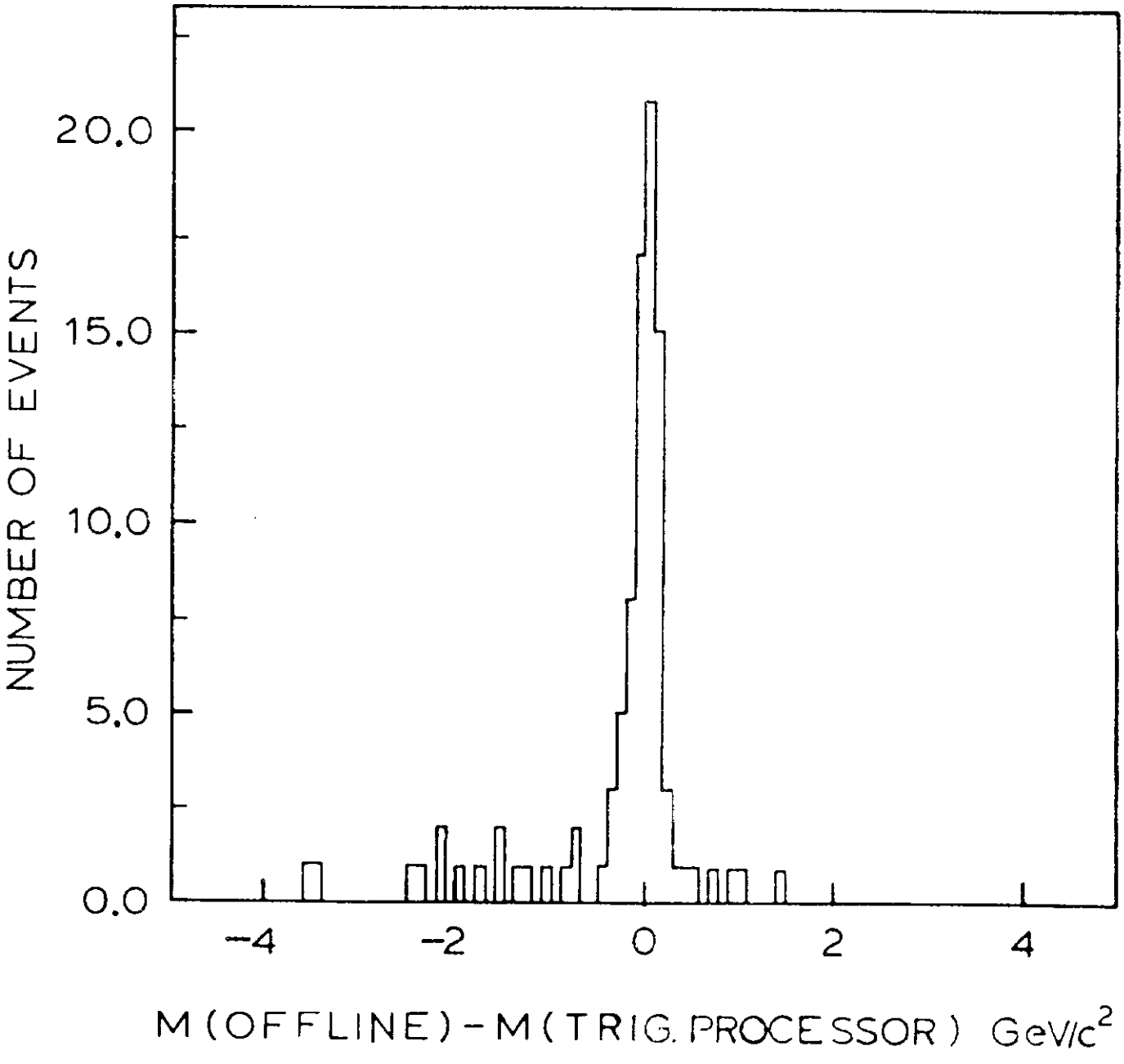
NUMBER OF EVENTS
20.0
15.0
10.0
5.0
0.0
−4
−2
0
2
4
M (OFFLINE) − M (TRIG. PROCESSOR) GeV/c²

Fig. 10

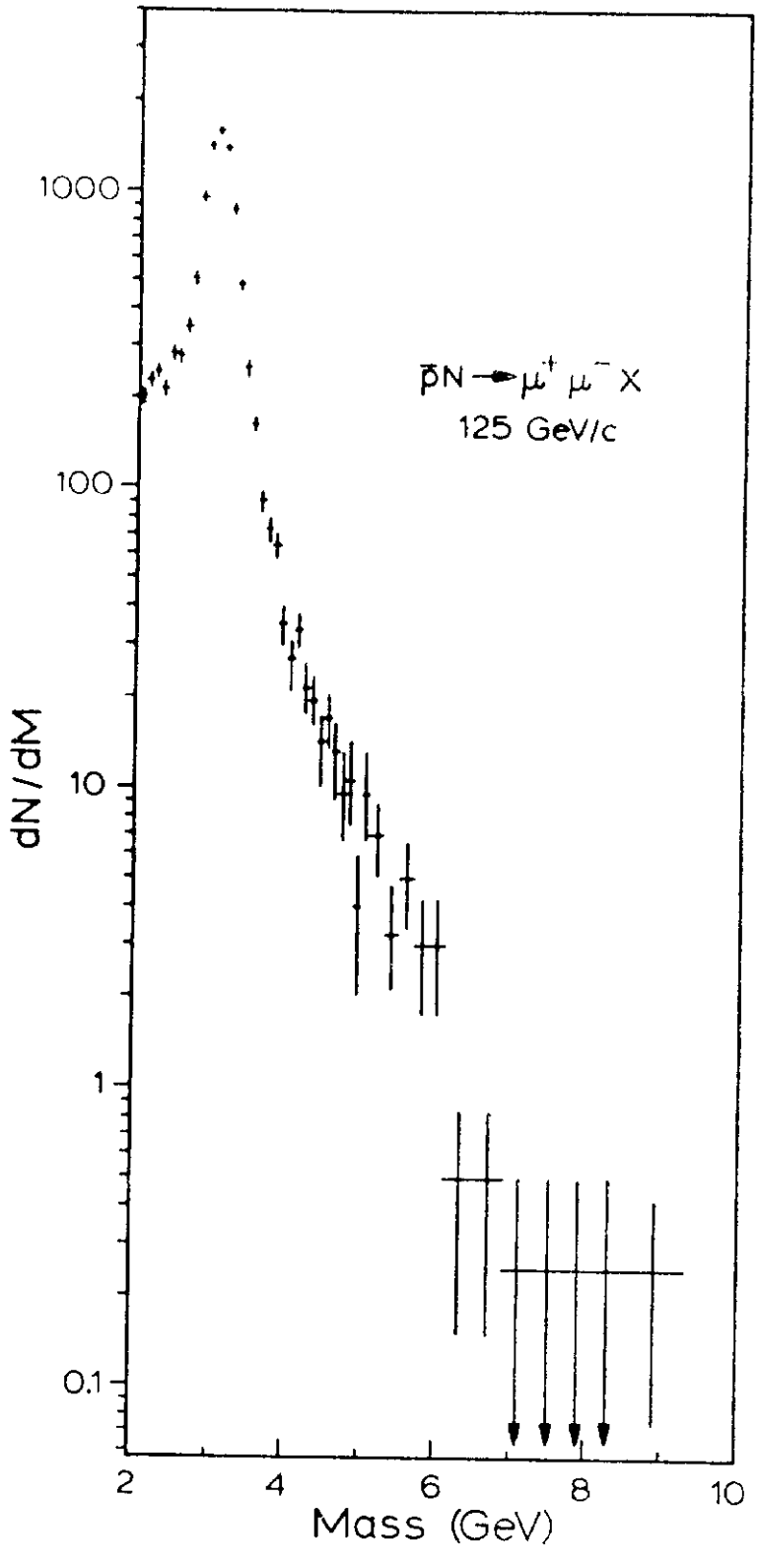
1000
100
10
1
0.1
dN/dM
$\bar{p}N \rightarrow \mu^+ \mu^- X$
125 GeV/c
2
4
6
8
10
Mass (GeV)

Fig. 11